

AMENDMENTS TO THE CLAIMS

Claims 1-2 (Cancelled)

3. (Currently Amended) ~~The adder of claim 2 wherein~~ An adder circuit comprising:

a first adder cell having:

a first logic gate having a first input that receives a first input signal, a second input that receives a second input signal, and a first output that generates a first logic signal, the first input signal, the second input signal, and the first logic signal each having a logic state, the first logic gate generating the first logic signal in response to the logic states of the first and second input signals, the first logic gate generating an inverted first input signal in response to the first input signal;

a first inverter circuit having a third input that receives a third input signal, a fourth input connected to receive the first logic signal, a first output that generates an inverted third signal, and a second output that generates an inverted first logic signal;

a first carry out circuit having a first control input connected to receive the first logic signal, a second control input connected to receive the inverted first logic signal, and an output, the carry out circuit including a first multiplexer that passes a first received signal to the output of the first carry out circuit when the first logic signal has a first logic state, and passes a second received signal to the output of the first carry out circuit when the first logic signal has a second logic state, the first received signal is being the first input signal; and

a first sum circuit having a first control input connected to receive the first logic signal, a second control input connected to receive the inverted first logic signal, a first sum input connected to the third input signal, a second sum input

connected to the inverted third signal, and an output, the second sum input and the output of the first sum circuit not be directly connected together.

4. (Cancelled)

5. (Currently Amended) The adder of claim 2 3 wherein the second received signal is the third input signal.

Claims 6-7 (Cancelled)

8. (Currently Amended) The adder of claim 2 3 wherein the first sum circuit includes a second multiplexer that passes a third received signal to the output of the first sum circuit when the logic signal has a first logic state, and passes a fourth received signal to the output of the first sum circuit when the logic signal has a second logic state.

9. (Original) The adder of claim 8 wherein the third received signal is the third input signal, an input to the second multiplexer being connected to the first sum input.

Claims 10-11 (Cancelled)

12. (Original) The adder of claim 8 wherein the fourth received signal is the inverted third signal.

13. (Cancelled)

14. (Currently Amended) The adder of claim ± 3 and further comprising a first buffering inverter having an input connected to the output of the first carry out circuit, and an output.

Claims 15-16 (Cancelled)

17. (Currently Amended) The adder circuit of claim ± 3 wherein the output of the first carry out circuit has a first active state; and further comprising:

a second adder cell connected to receive a signal from the output of the first carry out circuit of the first adder cell, the second adder cell having:

a second logic gate having a fifth input that receives a fifth input signal, a sixth input that receives a sixth input signal, and a second output that generates a second logic signal, the fifth input signal, the sixth input signal, and the second logic signal each having a logic state, the second logic gate generating the second logic signal in response to the logic states of the fifth and sixth input signals, the second logic gate generating an inverted fifth signal in response to the fifth input signal;

a second inverter circuit having a seventh input that receives a seventh input signal, an eighth input connected to receive the second logic signal, a first output that generates an inverted seventh signal, and a second output that generates an inverted second logic signal;

a second carry out circuit having a first control input connected to receive the second logic signal, a second control input connected to receive the inverted second logic signal, and a second output, the second carry out circuit including a second multiplexer that passes a third received signal to the output of the second carry out circuit when the first logic signal has a first logic state, and passes the signal from the output of the first carry out circuit to the output of the

second carry out circuit when the first logic signal has a second logic state, the second output of the second carry out circuit having a second active state opposite the first active state; and

a second sum circuit having a first control input connected to receive the second logic signal, a second control input connected to receive the inverted second logic signal, and an output.

18. (Currently Amended) The adder circuit of claim ~~17~~ and 17 and further comprising:

a third adder cell connected to receive a signal from the output of the second carry out circuit of the second adder cell, the third adder cell having:

a third logic gate having an ninth input that receives a ninth input signal, a tenth input that receives a tenth input signal, and a third output that generates a third logic signal, the ninth input signal, the tenth input signal, and the third logic signal each having a logic state, the third logic gate generating the third logic signal in response to the logic states of the ninth and tenth input signals, the third logic gate generating an inverted ninth signal in response to the ninth input signal;

a third inverter circuit having a eleventh input that receives an eleventh input signal, a twelfth input connected to receive the third logic signal, a first output that generates an inverted third signal, and a second output that generates an inverted third logic signal;

a third carry out circuit having a first control input connected to receive the third logic signal, a second control input connected to receive the inverted third logic signal, and a second output, the second output of the third carry out circuit having a second active state; and

a third sum circuit having a first control input connected to receive the third logic signal, a second control input connected to receive the inverted third logic signal, and an output.

19. (Original) The adder circuit of claim 17 wherein the first adder cell is in a first row and the second adder cell is in a second row.

20. (Original) The adder circuit of claim 18 wherein the first adder cell is in a first row, the second adder cell is in a second row, and the third adder cell is in a third row.

Claims 21-22 (Cancelled)

23. (Currently Amended) The circuit of claim ~~1~~ 5 wherein the first logic gate is an XOR gate when the first input signal and the second input signal have equivalent signal polarities.

24. (Currently Amended) The circuit of claim ~~1~~ 5 wherein the first logic gate is an XOR gate when the first input signal and the second input signal have different signal polarities.

25. (New) An adder circuit comprising:
a first adder cell having:
an exclusive OR circuit having a first input, a second input, an exclusive OR output, and a first signal output;
a first output circuit having:
a first transmission gate having a first input connected to the first signal output, a first gate, a second gate, and a first output;

a second transmission gate having a second input, a third gate connected to the second gate, a fourth gate, and a second output connected to the first output;

a third transmission gate having a third input, a fifth gate connected to the fourth gate, a sixth gate, and a third output;

a fourth transmission gate having a fourth input, a seventh gate connected to the sixth gate, an eighth gate, and a fourth output connected to the third output; and

an inverter having an input connected to the third input of the third transmission gate, and an output connected to the fourth input of the fourth transmission gate.

26. (New) The adder circuit of claim 25 wherein the first input of the first transmission gate is connected to the first input of the exclusive OR gate.

27. (New) The adder circuit of claim 26 wherein the second input of the second transmission gate is connected to the input of the inverter.

28. (New) The adder circuit of claim 27 wherein the first gate, the fourth gate, the fifth gate, and the eighth gate are connected together.

29. (New) The adder circuit of claim 28 and further comprising an inversion circuit having an input connected to the exclusive OR output, and an output connected to the first gate.

30. (New) The adder circuit of claim 26 and further comprising:
a second adder cell having:

an exclusive OR circuit having a first input, a second input, an exclusive OR output, and a second signal output;
a second output circuit having:
a fifth transmission gate having a fifth input connected to the second signal output, a ninth gate, a tenth gate, and a fifth output; and
a sixth transmission gate having a sixth input, an eleventh gate connected to the tenth gate, a twelfth gate, and a sixth output connected to the fifth output, the sixth input being connected to the first output of the first transmission gate of the first output circuit.

31. (New) The adder circuit of claim 26 and further comprising
an inverting circuit having an input connected to the first output of the first transmission gate of the first output circuit; and
a second adder cell having:
an exclusive OR circuit having a first input, a second input, an exclusive OR output, and a second signal output;
a second output circuit having:
a fifth transmission gate having a fifth input connected to the second signal output, a ninth gate, a tenth gate, and a fifth output; and
a sixth transmission gate having a sixth input, an eleventh gate connected to the tenth gate, a twelfth gate, and a sixth output connected to the fifth output, the sixth input being connected to the output of the inverting circuit.

32. (New) The adder of claim 25 wherein:
the exclusive OR gate includes an inverting circuit that has an input connected to the first input of the exclusive OR gate, and an output; and
the first input of the first transmission gate is connected to the output of the inverting circuit.

33. (New) The adder of claim 32 wherein the second input of the second transmission gate is connected to the output of the inverter.

34. (New) The adder of claim 33 wherein the first gate, the fourth gate, the fifth gate, and the eighth gate are connected together.

35. (New) The adder of claim 34 and further comprising an inversion circuit having an input connected to the exclusive OR output, and an output connected to the first gate.

36. (New) The adder circuit of claim 32 and further comprising
an inverting circuit having an input connected to the first output of the first transmission gate of the first output circuit; and

a second adder cell having:

an exclusive OR circuit having a first input, a second input, an exclusive OR output, and a second signal output;

a second output circuit having:

a fifth transmission gate having a fifth input connected to the second signal output, a ninth gate, a tenth gate, and a fifth output; and

a sixth transmission gate having a sixth input, an eleventh gate connected to the tenth gate, a twelfth gate, and a sixth output connected to the fifth output, the sixth input being connected to the output of the inverting circuit.